101

SVKM's NMIMS
MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING

Programme: B.Tech/ MBA Tech (IT) Year: II Semester: III

Academic Year: 2019-20

Subject: Digital Logic Design

Date: 12 November 2019

Marks: 70
Time: 2.00 pm - 5.00 pm
Durations: 3 (Hrs)
No. of Pages: 2

Re-examination B.Tech/ MBA Tech (2018-19) / MBA Tech (2017-18)

Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover of the Answer Book, which is provided for their use.

1) Question No. _1___ is compulsory.
2) Out of remaining questions, attempt any __4___ questions.
3) **In all ___5_ questions to be attempted.**
4) All questions carry equal marks.
5) **Answer to each new question to be started on a fresh page.**
6) **Figures in brackets on the right hand side indicate full marks.**
7) **Assume suitable data if necessary.**

1. Perform the following:
   a) Convert the hexadecimal number 68BE to binary and then from binary convert it to octal. [2]
   b) Represent $(4096)_{10}$ in BCD code and excess-3 code. [2]
   c) Write the Excitation table and characteristic equation of JK flip flop. [2]
   d) Using 2's complement perform $(23)_{10} - (48)_{10}$. [2]
   e) Compare combinational circuits and sequential circuits. [3]
   f) What is race around condition? [3]

2. a) Draw the logic circuit for the given Boolean equation. Simplify the circuit using Boolean algebra and draw the simplified circuit. [6]

$$Y = \overline{(AB)} \cdot \overline{(B + C)}$$

   b) Simplify the following Boolean equation using Quine-Mc-Cluskey Method and verify with K-map. $F(A,B,C,D) = \sum m(2,3,7,9,11,13) + d(1,10,15)$ [8]

3. a) Simplify the following using K-Map. [7]

   i. $F(A,B,C,D) = \sum m(0,3,5,7,8,11,12,15) + d(2,13)$

   ii. $F(A,B,C,D) = \prod M(1,3,5,6,7,10,11) \cdot d(2,4)$

   b) Design BCD to excess-3 code converter. [7]

4. a) With the help of a neat block diagram explain the working of a JK Master-Slave flip-flop. [7]

   b) What is a decoder? Construct a 4×16 decoder with two 3×8 decoders. [7]

5. a) What is a multiplexer? Implement the following equation using 8:1 Multiplexer. [7]

   $F(A,B,C,D) = AB'CD + A'B'CD + AB'CD' + ABC'D + ABCD$

   b) Convert SR to D and T Flip flop. Draw the circuit. [7]

6. a) Design Mod-6 Ripple counter using JK flip flop. Write truth table and draw timing diagram. [7]

   b) What is a shift register? Explain the working of different types of shift registers. [7]

7. a) Explain working of PLA with block diagram. [5]
   b) Design full adder using two half adders. [5]
   c) Explain weighted and non-weighted binary codes. [4]